**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| Claim 1 | Accused Instrumentalities |
|---|---|
| A double-gate FinFET device, comprising: | Samsung provides a 10 nm bulk FinFET technology, which includes at least 10LPE, 10LPP and 10LPU.<br><br>After successful offering of 14nm FinFET technology, Samsung foundry has developed 10nm FinFET technology with more optimized fin structure and cost effective multi-patterning technology to meet aggressive market requirement.<br><br>. . . .<br><br>In order to support long-lived technology, design enablement and IP optimization has been built by collaborating with ecosystem partners. Collaboration specifically around optimal Fin-based design infrastructure and advanced IP development on top of 14nm learning has resulted in more competitive foundation libraries and advanced IP suite.<br><br>Samsung's 10nm FinFET Process Offering – 10LPE/10LPP/10LPU<br><br>10LPE(early Edition) targets the early technology leaders and time-to-market customers with such as mobile application SoCs to meet the latest mobile gadgets' aggressive schedule and improved performance/power requirement than 14nm. Foundry industry first mass production had started based on 10LPE with successful ramp up to support customer's product roadmap.<br><br>10LPP(Performance boosted version) is the 2nd generation 10nm FinFET technology with performance enhancement by 10% than 10LPE. Like as other FinFET technology, 10LPP is also single platform to cover wide application from high performance computing to low power mobile. 10LPP will be the right solution for 2018 or afet [*sic*] mass production.<br><br>10LPU is successful output of DTCO(Design Technology Co-Optimization) to offer more |

**EXHIBIT B**
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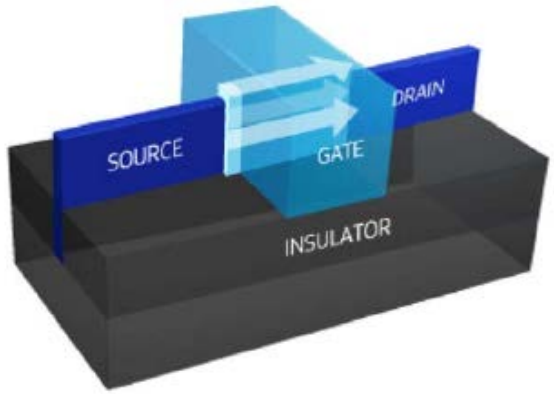
scalability and better performance than prior 10nm nodes. Technology qualification is scheduled at Sep., 2017.[1]

Samsung's 10 nm FinFET is illustrated below.[2]


Below is another illustration of the 10 nm FinFET.[3]




The 10 nm FinFET above exhibits a wrap-around gate structure similar to Samsung's 14 nm FinFET

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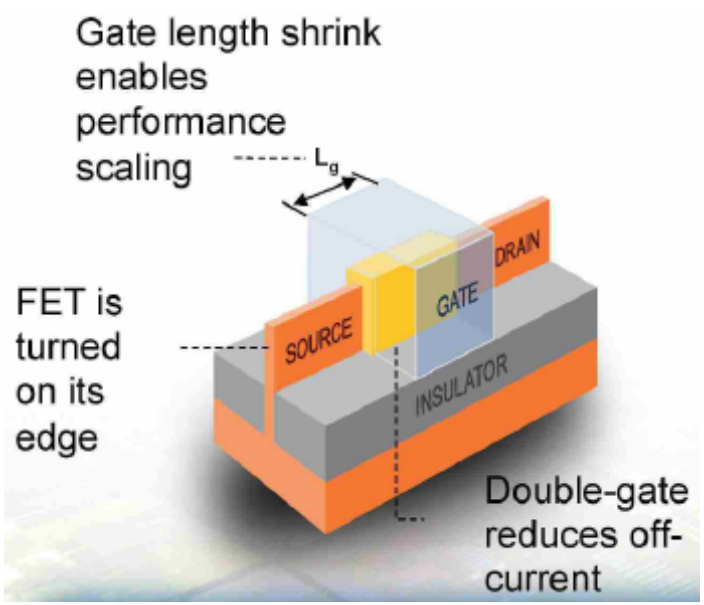
| | |
|---|---|
| | below.[4]<br>  <br><br>Qualcomm's Snapdragon 835 (MSM8998) is manufactured on at least Samsung's 10LPE.<br><br>"We are pleased to have the opportunity to work closely with Qualcomm Technologies in producing the Snapdragon 835 using our 10nm FinFET technology," said Jong Shik Yoon, executive vice president and head of foundry business, Samsung. "This collaboration is an important milestone for our foundry business as it signifies confidence in Samsung's leading chip process technology."<br><br>Snapdragon 835 is in production now and expected to ship in commercial devices in the first half of 2017.[5]<br><br>More specifically, the Snapdragon 835 chip was built on 300 nm wafers using the Samsung's 10LPE FinFET HKMG CMOS process.[6] |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

## Salient Features

- The Qualcomm Snapdragon 835 MSM8998 was built on 300 mm wafers using the Samsung's 10LPE FinFET HKMG CMOS process
- Gate pitch in the logic array is observed to be 68 nm
- SRAM gate pitch is observed to be 64 nm
- Gate length is found to be ~22 nm
- Logic fins are approximately 47 nm tall and the SRAM fins are about 50 nm tall
- Fin width is the same for NMOS and PMOS and is ~5 nm measured at the center of the fin height
- Logic fin pitch is approximately 42 nm
- Standard cell height is 420 nm (8.75 Track x 48 nm)
- Minimum metal 1 pitch is found to be 48 nm
- Minimum 6T-SRAM cell size is ~0.04 $\mu m^2$
- Cu metals 1 to 4 are found to have a Co liner and cap, while Cu metals 5 to 11 are found to be doped with Mn; all Cu metals have Ta-based liners
- An etch stop layer composed of AlNO is observed from above the trench contact up to the top of metal 3
- Self-aligned single dummy poly diffusion breaks are used

The Snapdragon 835 chip goes into the Samsung Galaxy S8 smartphones (models SM-G950U and SM-G955W).[7]

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

## Observed Critical Dimensions

| | |
|---|---|
| **Report code** | ACE-1704-802 |
| **Package dimensions** | 12.70 mm x 12.00 mm x 0.75 mm thick |
| **Manufacturer, part number, downstream** | Qualcomm, MSM8998, Samsung Galaxy S8 smartphones (models SM-G950U and SM-G955W) |
| **Wafer size, foundry, process type** | 300 mm, Samsung, 10 nm FinFET HKMG CMOS |
| **Die markings** | QUALCOMM<br>HG11-P2519-1 |
| **Die size (from die seal)** | 7.82 mm x 8.95 mm (69.99 $mm^2$) |
| **Die size (actual)** | 7.91 mm x 9.14 mm |
| **Number, type of metals** | 12, 11 Cu, 1 Al |
| **Contacted logic gate pitch** | 68 nm |
| **Minimum metal pitch** | 48 nm |
| **Logic fin pitch** | 42 nm |
| **Contacted SRAM gate pitch** | 64 nm |
| **Minimum SRAM cell size** | 0.128 µm x 0.315 µm (~0.04 $µm^2$) |
| **Minimum standard cell height** | 420 nm (8.75 track x 48 nm) |
| **Technology generation** | 10 nm "10LPE" |
| **Feature measured to determine process generation** | Minimum metal pitch relative to Samsung 14 nm "14LPP" |

The following is transmission electron microscopy ("TEM") image of the actual transistors in the Snapdragon 835 chip.[8]

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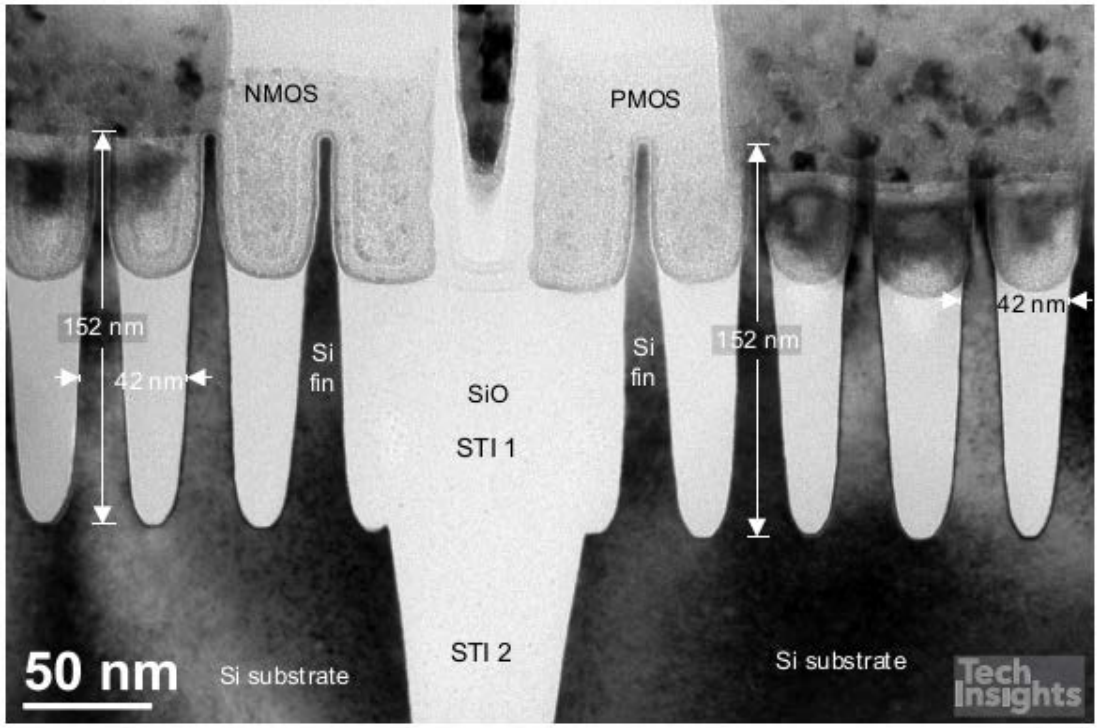
**Infringement Chart for U.S. Patent No. 6,885,055**




The following are additional TEM images of the 10 nm transistor.[9]

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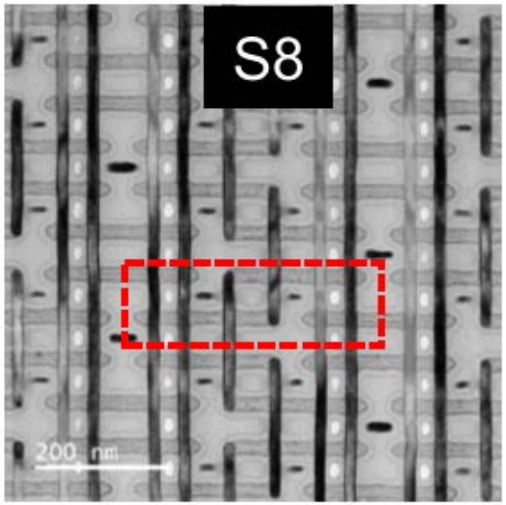
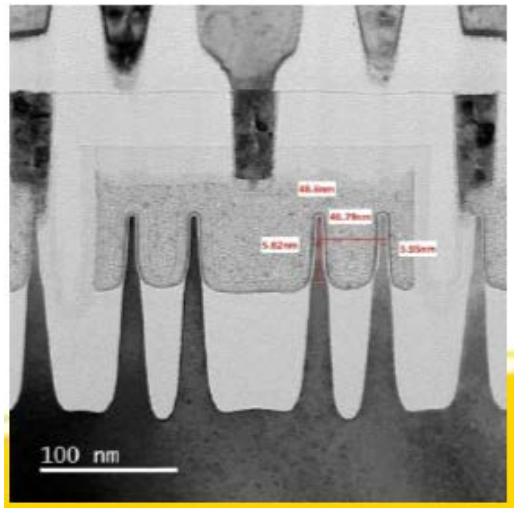
**Infringement Chart for U.S. Patent No. 6,885,055**




It is anticipated that discovery will provide further details of the manner of infringement of the 10 nm instrumentalities.

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

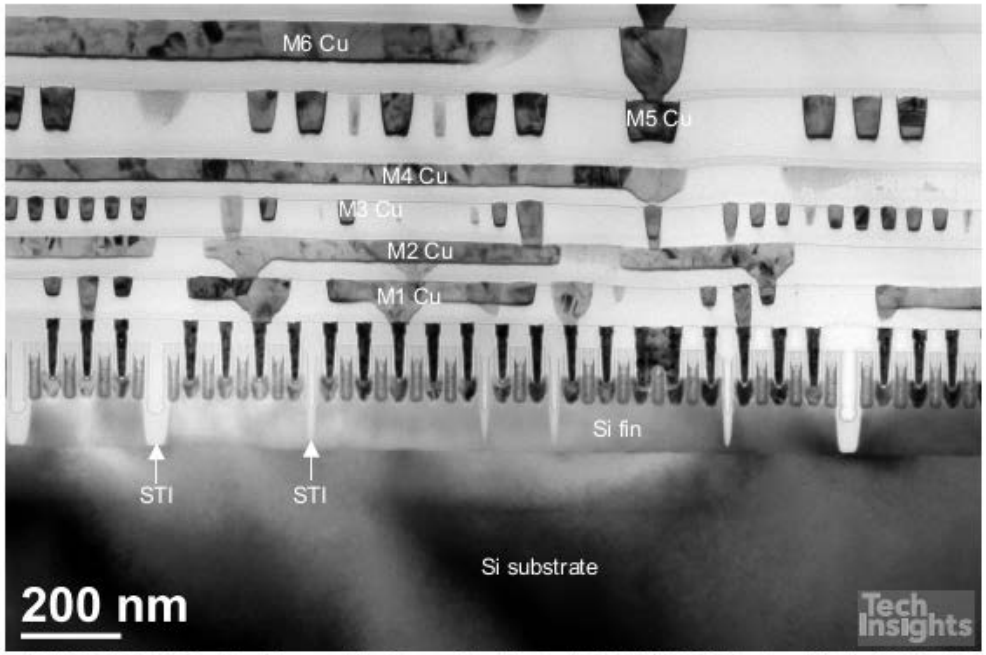
| | |
|---|---|
| a bulk silicon substrate; | The Accused Instrumentalities comprise a bulk silicon substrate.<br><br>This feature is shown in the following TEM image of the actual transistors in the Snapdragon 835.[10]<br><br>  <br>4.TEM/TEM X-Section/Across the Transistor Gates/LOGIC/PMOS/gates 14k_b_225177<br><br>The TEM shows a Si substrate. |
| a Fin active region which is a wall-shape single crystalline silicon on a surface of the bulk silicon substrate and connected to | The Accused Instrumentalities comprise a wall-shape single crystalline silicon Fin active region on a surface of the bulk silicon substrate and connected to the bulk silicon substrate.<br><br>These features are shown in the following TEM images of the actual transistors in the Snapdragon |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

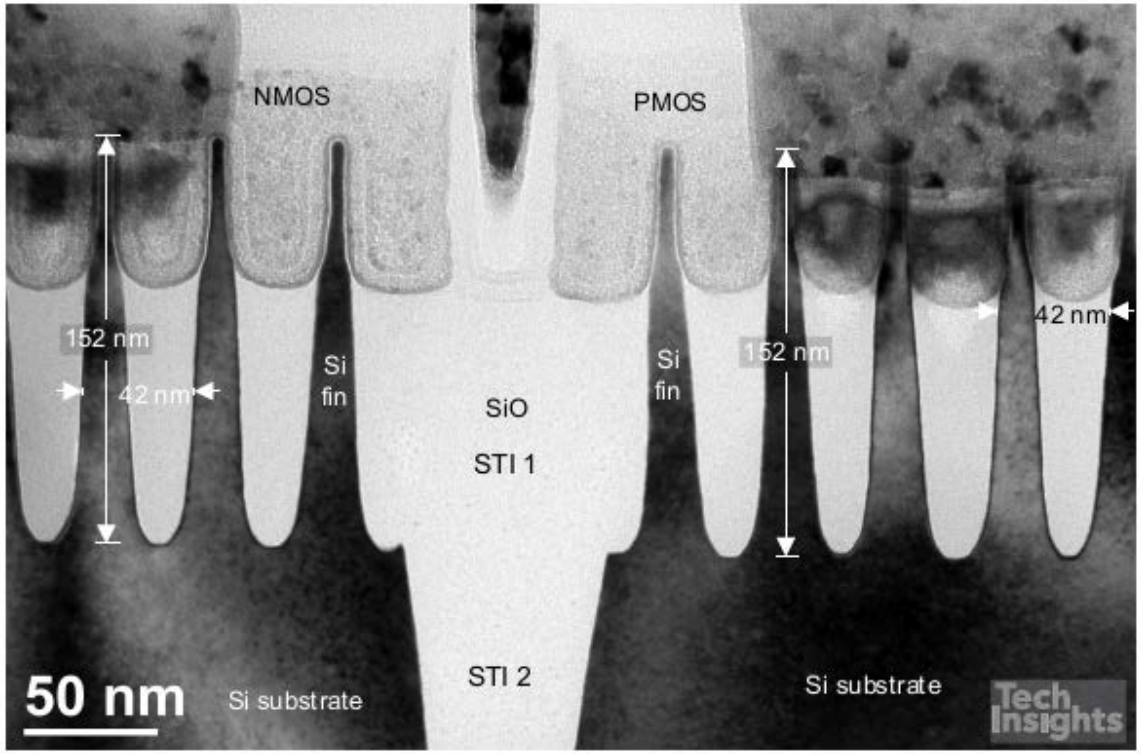
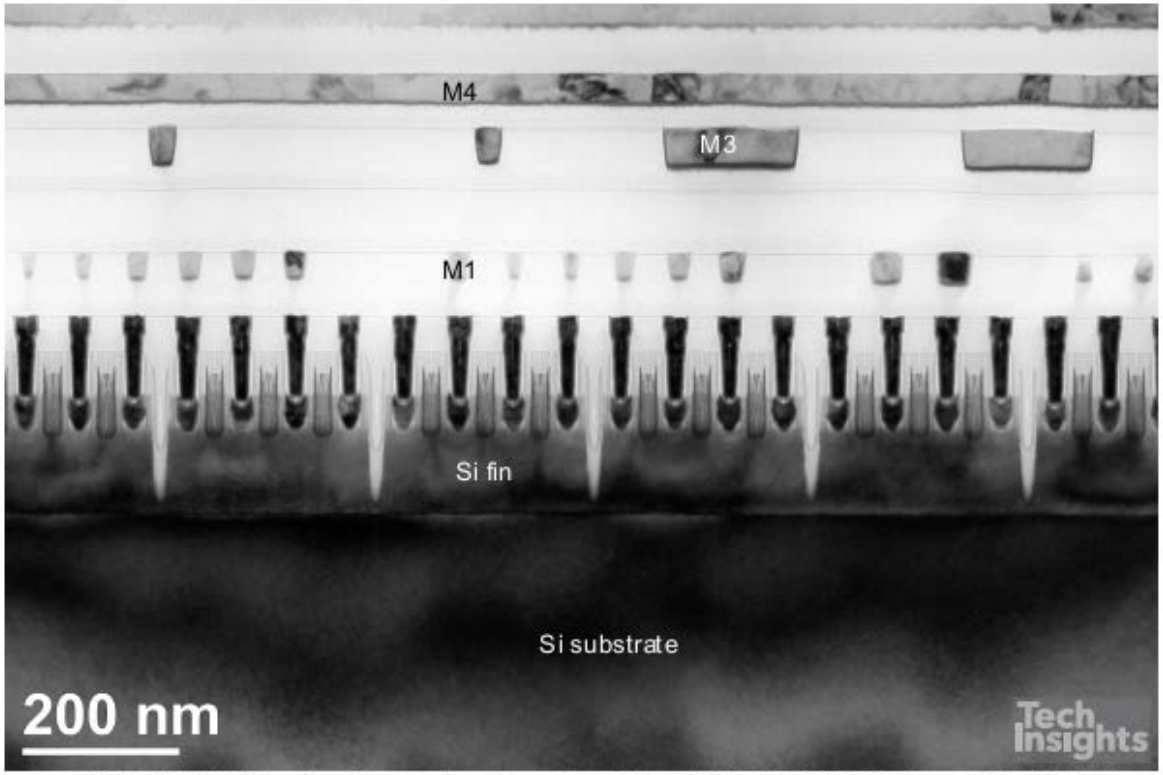
| | |
|---|---|
| said bulk silicon substrate; | 835.[11]<br>  <br><br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/n and pmos 64k_vg_225176<br><br>An additional TEM image is shown below:[12] |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**




4.TEM/TEM X-Section/Across the Transistor Gates/LOGIC/NMOS/Gates__18k_225177

The TEMs show a Si fin. The fin is wall-shape. It is single crystalline silicon. It is on a surface of the bulk silicon substrate. It is connected to the bulk silicon substrate.

**EXHIBIT B**
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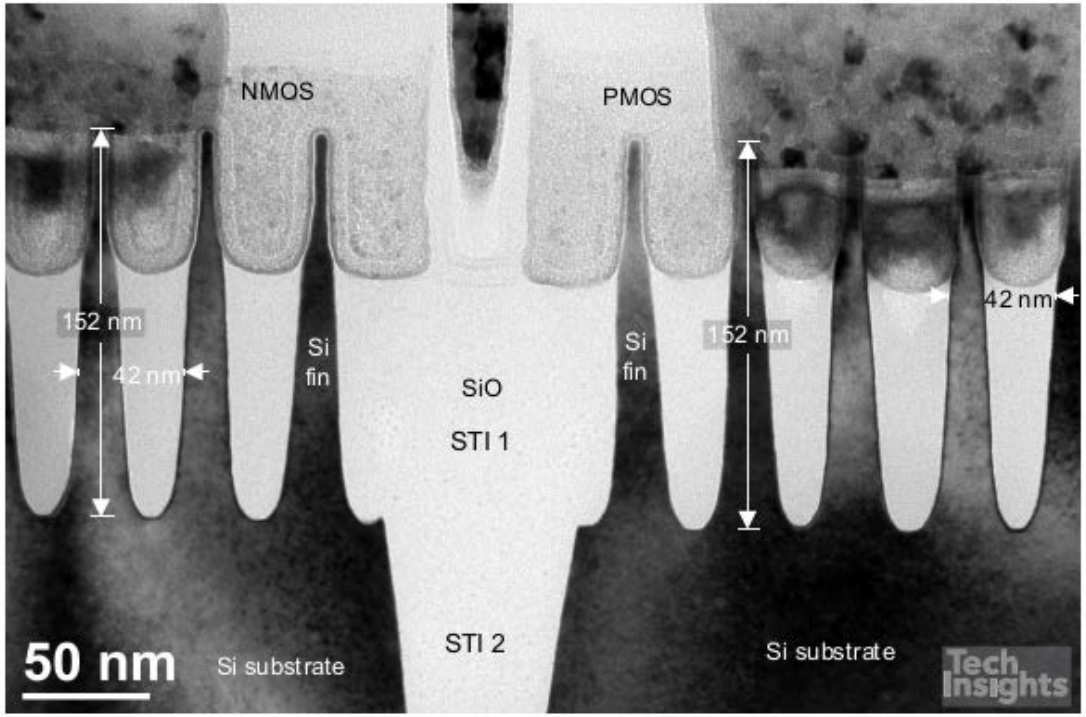
| | |
|---|---|
| a second oxide layer which is formed up to a certain height of the Fin active region from the surface of bulk silicon substrate; | The Accused Instrumentalities comprise a second oxide layer which is formed up to a certain height of the Fin active region from the surface of bulk silicon substrate.<br><br>These features are shown the following TEM image of the actual transistors in the Snapdragon 835.[13]<br><br>  <br><br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/n and pmos 64k_vg_225176<br><br>The TEM shows an SiO layer formed up to a certain height of the Fin active region from the substrate surface. |

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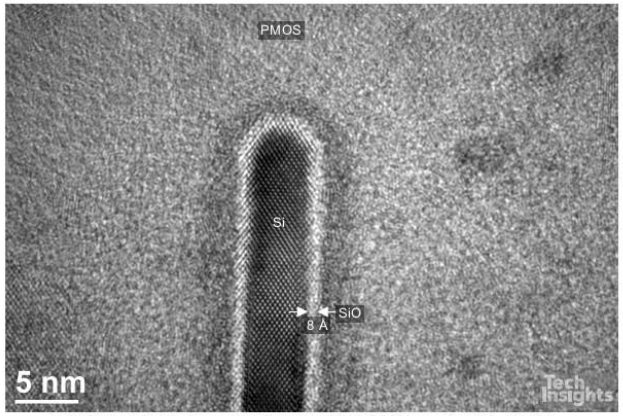
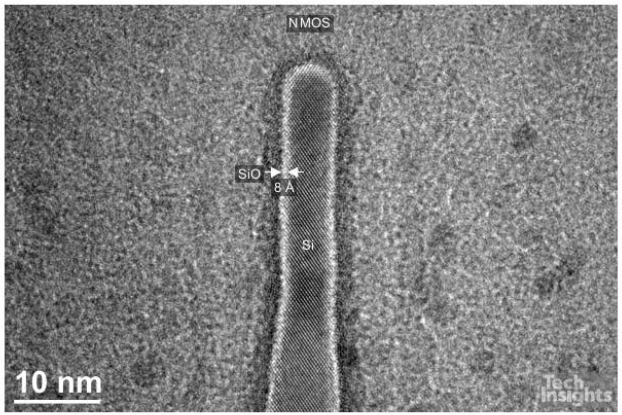
| | |
|---|---|
| a gate oxide layer which is formed on both side-walls of the Fin active region protruded from said second oxide layer; | The Accused Instrumentalities comprise a gate oxide layer which is formed on both side-walls of the Fin active region, protruded from said second oxide layer.<br><br>These features are shown in the following TEM images of the actual transistors in the Snapdragon 835.[14]<br><br>**Cross-Sectional View**<br>  <br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/pmos fin 530k_225176<br>  <br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/nmos 360k g_225176<br><br>The TEMs show the gate oxide formed on both side-walls of the Fin active region. |

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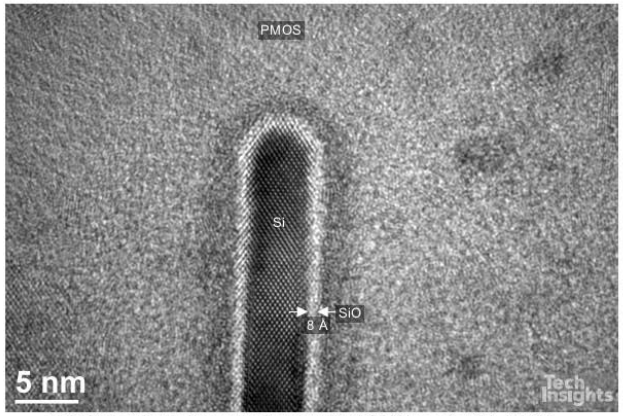
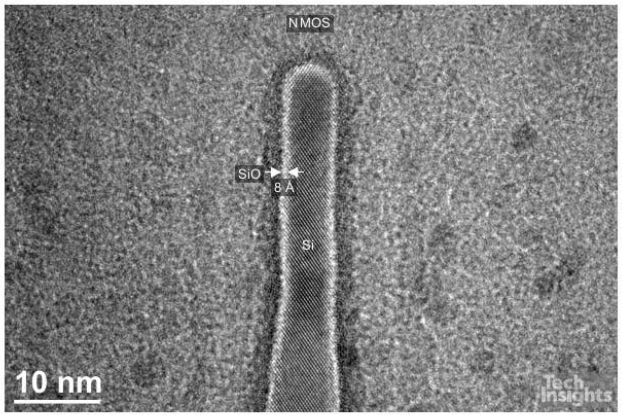
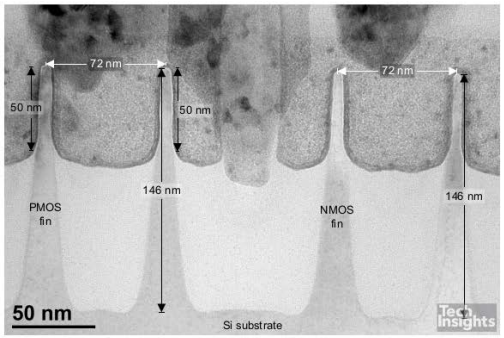
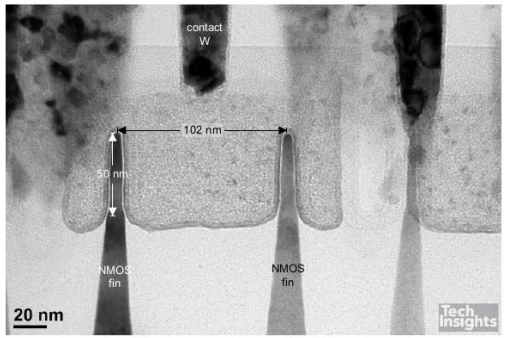
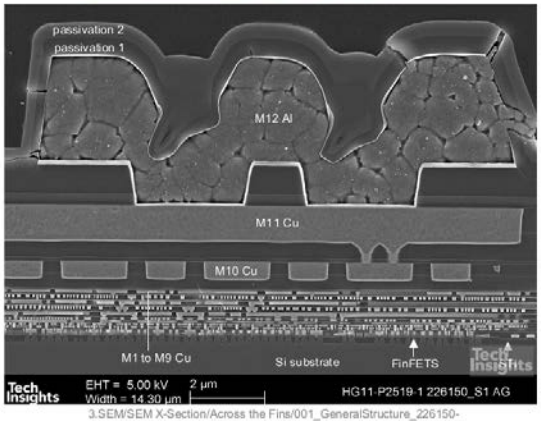
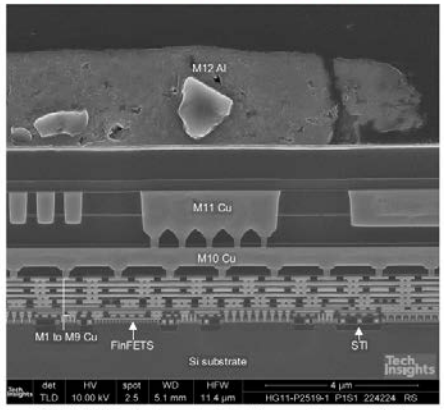
| | |
|---|---|
| a first oxide layer which is formed on the upper surface of said Fin active region with a thickness greater or equal to that of the gate oxide; | The Accused Instrumentalities comprise a first oxide layer which is formed on the upper surface of the Fin active region with a thickness greater or equal to that the gate oxide.<br><br>These features are show in the following TEM images of the actual transistors in the Snapdragon 835.[15]<br><br>**Cross-Sectional View**<br>  <br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/pmos fin 530k_225176<br>  <br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/nmos 360k g_225176<br><br>The TEMS show a SiO layer formed on the upper surface of the fin. The first oxide layer has a thickness greater or equal to that of the gate oxide. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| | |
|---|---|
| a gate which is formed on said first and second oxide layer; | The Accused Instrumentalities comprise a gate, which is formed on the first and second oxide layers.<br><br>These features are shown in the following TEM images of the actual transistors in the Snapdragon 835.[16]<br><br>  <br><br>4.TEM/TEM X-Section/Across the Transistor Fins/SRAM/pnnp sram fins 88k g2_241052<br><br>  <br><br>4.TEM/TEM X-Section/Across the Transistor Fins/SRAM/sram nmos 88k_c_241052<br><br>Cross Section View – Across the Fins<br><br>  <br><br>3.SEM/SEM X-Section/Across the Fins/001_GeneralStructure_226150-<br><br>Cross Section View – Across the Gates<br><br>  <br><br>3.SEM/SEM X-Section/Across the Gates/09_general_structure_224224<br><br>The TEMs show a gate. It is formed on the first and second oxide layers. |

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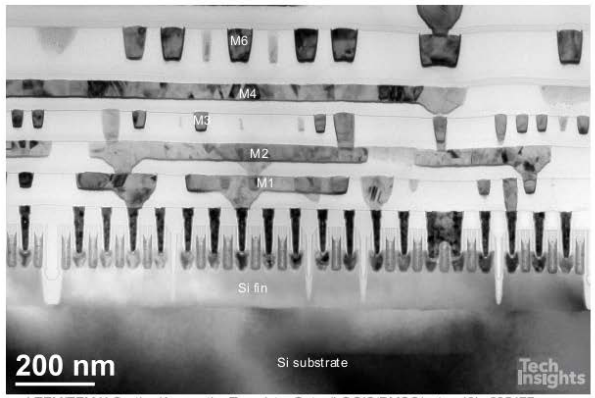
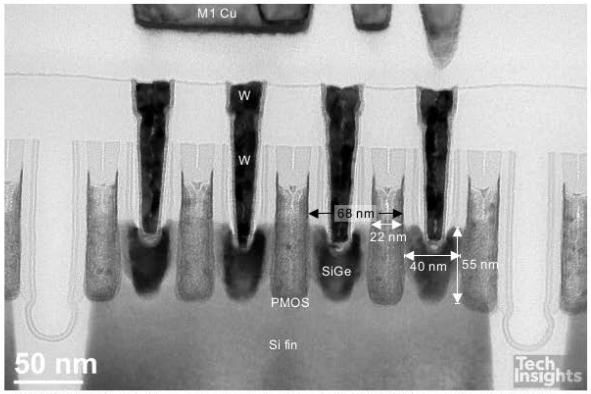
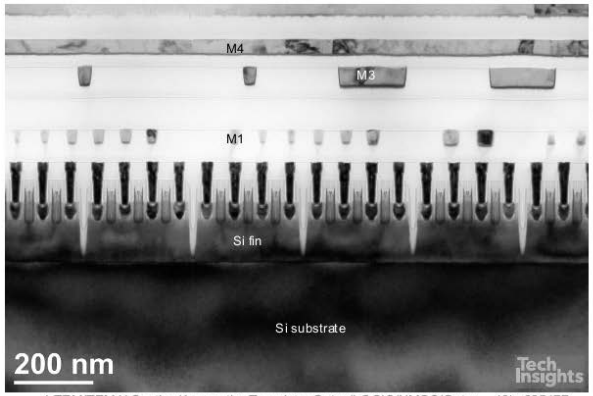
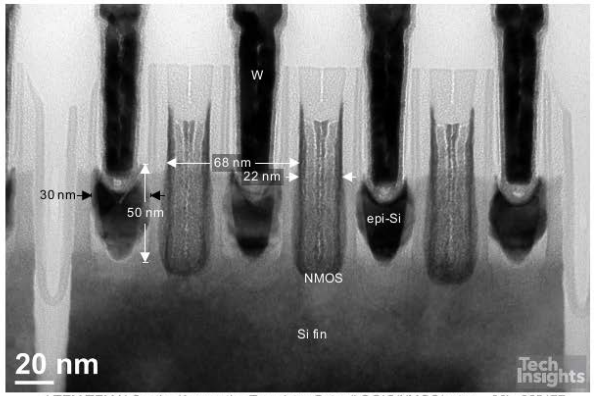
| | |
|---|---|
| a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region; and | The Accused Instrumentalities comprise a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region.<br><br>These features are show in the following TEM images of the actual transistors in the Snapdragon 835.[17]<br><br>  <br>4.TEM/TEM X-Section/Across the Transistor Gates/LOGIC/PMOS/gates 18k_225177<br><br>  <br>4.TEM/TEM X-Section/Across the Transistor Gates/LOGIC/PMOS/gates 64k_g4_225177<br><br>  <br>4.TEM/TEM X-Section/Across the Transistor Gates/LOGIC/NMOS/Gates__18k_225177<br><br>  <br>4.TEM/TEM X-Section/Across the Transistor Gates/LOGIC/NMOS/gates__88k_225177<br><br>The TEMs show a source/drain region. That region is formed on both sides of the Fin active region |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

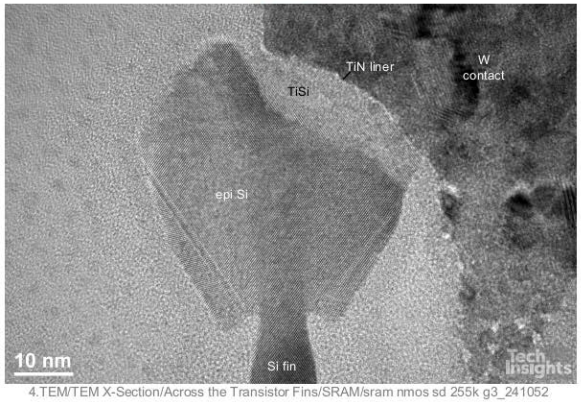
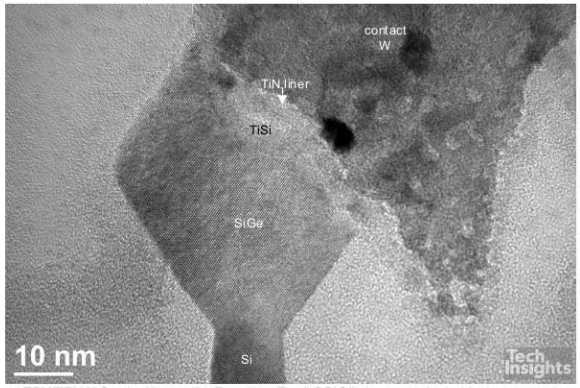
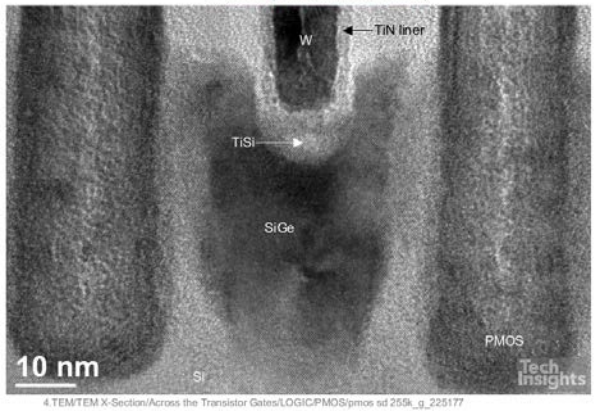
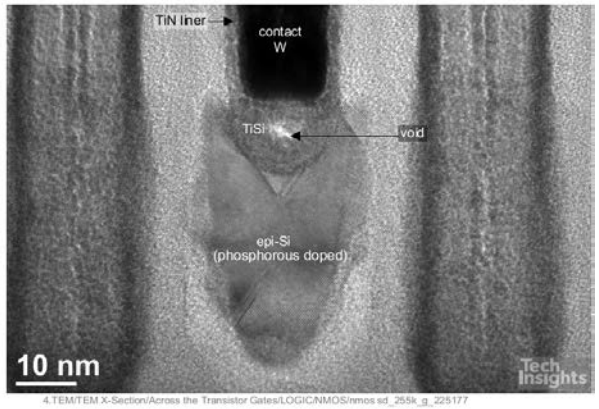
| | |
|---|---|
| | except where the gate overlaps with the Fin active region. |
| a contact region and a metal layer which are formed at said source/drain and gate contact region, | The Accused Instrumentalities comprise a contact region and a metal layer which are formed at said source/drain and gate contact region.<br><br>These features are shown in the following TEM images of the actual transistors in the Snapdragon 835.[18]<br><br>NMOS<br>  <br>4.TEM/TEM X-Section/Across the Transistor Fins/SRAM/sram nmos sd 255k g3_241052<br><br>PMOS<br>  <br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/between the logic blocks_pmos sd<br><br>PMOS (Across the Gates)<br>  <br>4.TEM/TEM X-Section/Across the Transistor Gates/LOGIC/PMOS/pmos sd 255k_g_225177<br><br>NMOS (Across the Gates)<br>  <br>4.TEM/TEM X-Section/Across the Transistor Gates/LOGIC/NMOS/nmos sd_255k_g_225177 |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| | |
|---|---|
| | The TEMs show a contact region and a metal layer formed at the source/drain and gate contact region. |
| wherein the thickness of said gate oxide layer is between 0.5 nm and 10 nm, and the thickness of said first oxidation layer is between 0.5 nm and 200 nm. | In the Accused Instrumentalities, the thickness of the gate oxide layer is between 0.5nm and 10nm, and the thickness of the first oxidation layer is between 0.5 nm and 200 nm.<br><br>These features are shown in the following TEM images of the actual transistors in the Snapdragon 835.[19] |

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## PMOS and NMOS Gate and Epi Dimensions

**PMOS**

| Structure | Size (nm) |
|---|---|
| Gate length | ~22 |
| PMOS gate fill TiAlC thickness | ~3.7 |
| PMOS WF metal (TiN) thickness | ~3.1 |
| PMOS TaN thickness | ~1.5 |
| PMOS TiN cap thickness | ~0.8 |
| PMOS logic gate dielectric thickness ($HfO_2/SiO_2$) | ~2.5 (1.7/0.8) |
| PMOS source/drain SiGe epi thickness/width | ~55/40 |

**NMOS**

| Structure | Size (nm) |
|---|---|
| Gate length | ~22 |
| NMOS gate fill TiN thickness | ~3 |
| NMOS WF metal (TiAlC) thickness | ~4.1 |
| NMOS TaN thickness | ~1.5 |
| NMOS TiN cap thickness | ~0.7 |
| NMOS logic gate dielectric thickness ($HfO_2/SiO_2$) | ~2.5 (1.7/0.8) |
| NMOS source/drain Si epi thickness/width | ~50/30 |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

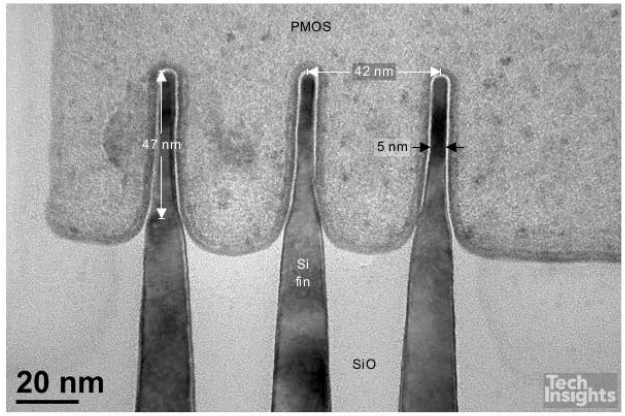
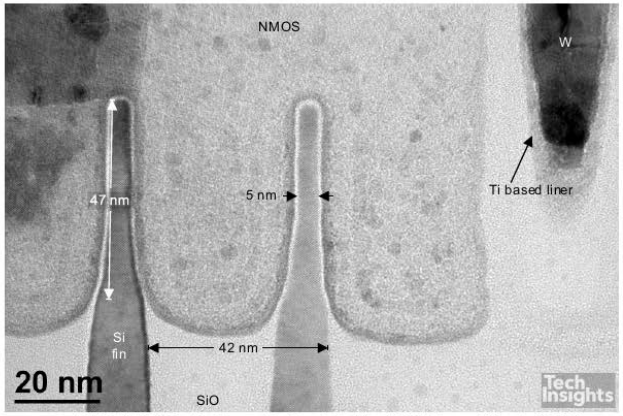
| Claim 2 | Accused Instrumentalities |
|---|---|
| The device as claimed in claim 1, wherein the width of said Fin active region lies in a range between 4 nm and 100 nm. | The Accused Instrumentalities comprise a FinFET device, as claimed in claim 1, wherein the width of said Fin active region lies in a range between 4 nm and 100 nm.<br><br>For example, in the Qualcomm Snapdragon 835, the width of the Fin active region lies in a range between 4 nm and 100 nm.[20]<br><br>▪ Fin width is the same for NMOS and PMOS and is ~5 nm measured at the center of the fin height<br><br>This is shown in the images below.[21]<br><br>PMOS<br>  <br><br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/pmos fins 130k_225176<br><br>NMOS<br>  <br><br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/nmos 180k g2_225176 |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

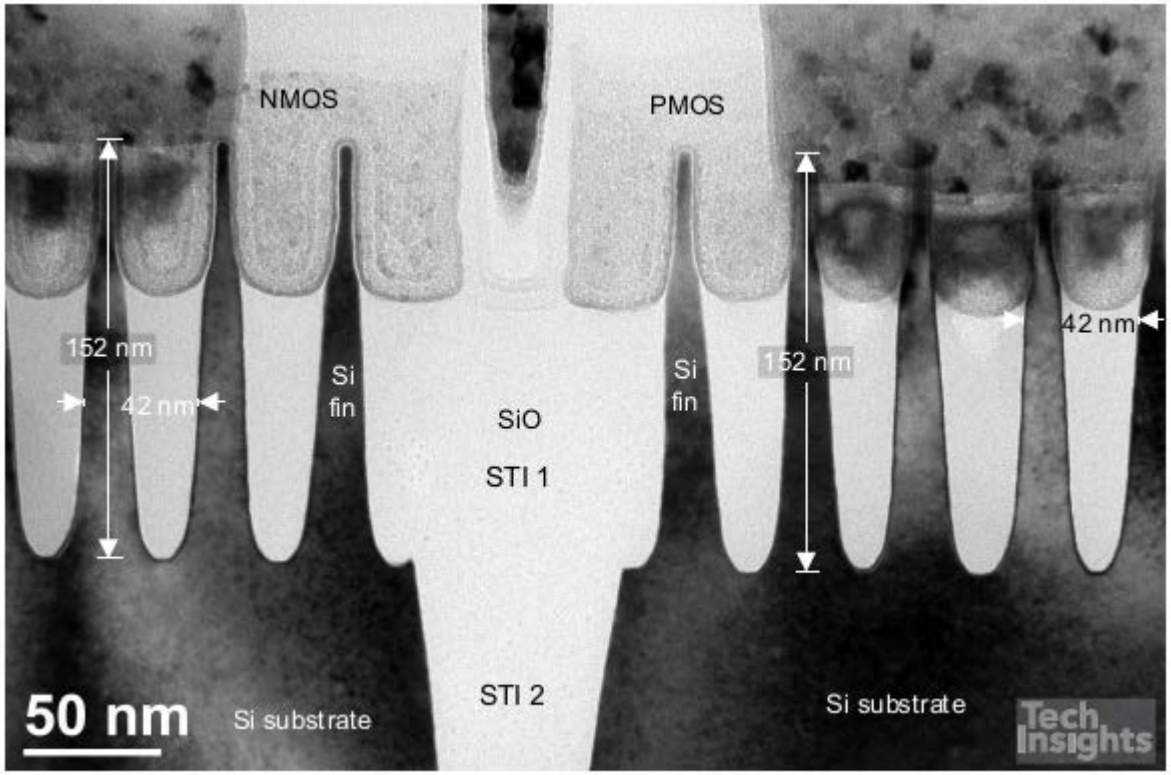
| Claim 3 | Accused Instrumentalities |
|---|---|
| The device as claimed in claim 1, wherein the height of said Fin active region from the surface of said bulk silicon substrate lies in a range between 10 nm and 1000 nm. | The Accused Instrumentalities comprise a FinFET device, as claimed in claim 1, wherein the height of the Fin active from the surface of the bulk silicon substrate lies in a range between 10nm and 1000nm.<br><br>For example, in the Qualcomm Snapdragon 835, the height of the Fin active region from the surface of the bulk silicon substrate lies in a range between 10nm and 1000nm, as shown below.[22]<br><br>  <br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/n and pmos 64k_vg_225176 |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

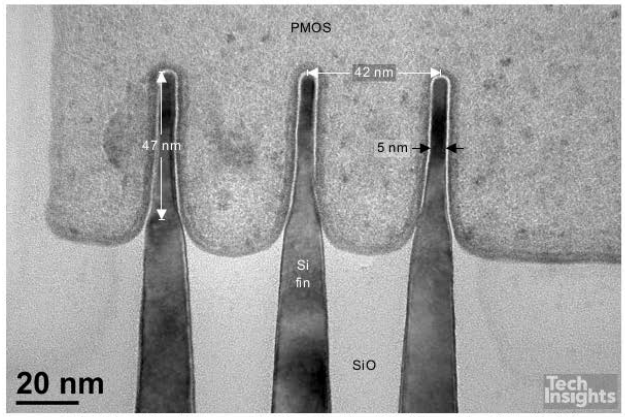
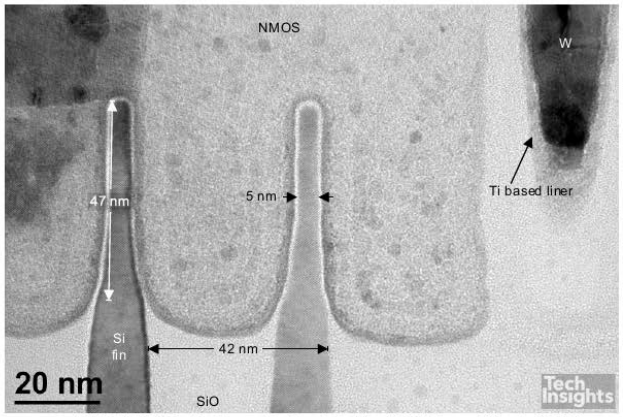
| Claim 4 | Accused Instrumentalities |
|---|---|
| The device as claimed in claim 3, wherein the height of said Fin active region from the surface of said second oxide layer is between 5 nm and 300 nm. | The Accused Instrumentalities comprise a FinFET device, as claimed in claim 3, wherein the height of the Fin active region from the surface of the second oxide layer is between 5 nm and 300 nm.<br><br>For example, as shown below, in the Qualcomm Snapdragon 835, the height of the Fin active region from the surface of the second oxide layer is between 5 nm and 300 nm:[23]<br><br>▪ Logic fins are approximately 47 nm tall and the SRAM fins are about 50 nm tall<br><br>This is shown in the images below:[24]<br><br>PMOS<br>  <br><br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/pmos fins 130k_225176<br><br>NMOS<br>  <br><br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/nmos 180k g2_225176 |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

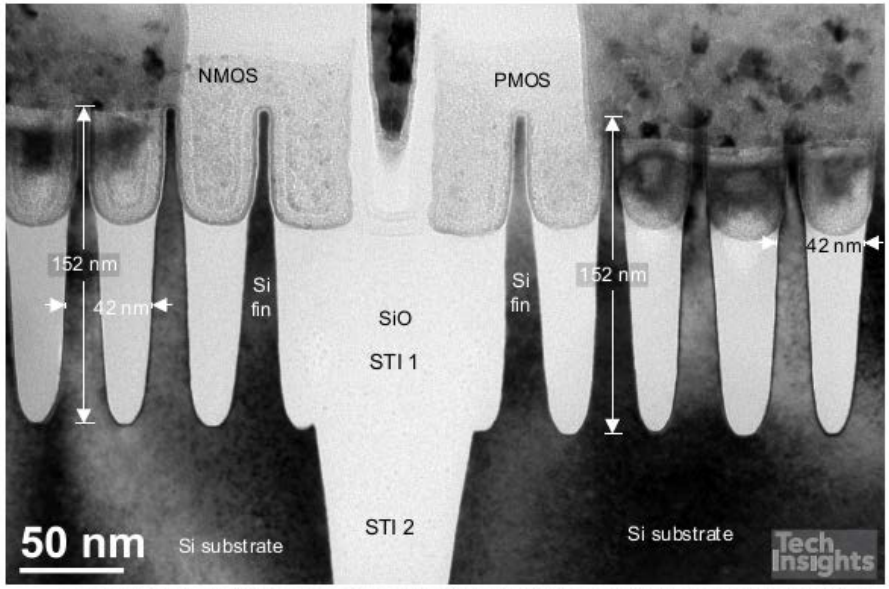
| Claim 5 | Accused Instrumentalities |
|---|---|
| The device as claimed in claim 1, wherein the parasitic capacitance between said gate and bulk silicon substrate is reduced by selecting the thickness of said second oxidation layer to be between 20 nm and 800 nm. | The Accused Instrumentalities comprise a FinFET device, as claimed in claim 1, wherein the parasitic capacitances between the gate and bulk silicon substrate is reduced by selecting the thickness of the second oxidation layer to be between 20 nm and 800 nm.<br><br>For example, in the Qualcomm Snapdragon 835, the thickness of the second oxidation layer is selected to be between 20 nm and 800 nm, reducing the parasitic capacitance between the gate and bulk silicon substrate. The second oxidation layer thickness is between 20 nm and 800 nm as shown below:[25]<br><br>  <br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/n and pmos 64k_vg_225176<br><br>This design in the Samsung 10nm FinFET technology reduces the parasitic capacitance between the gate and the bulk silicon substrate. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

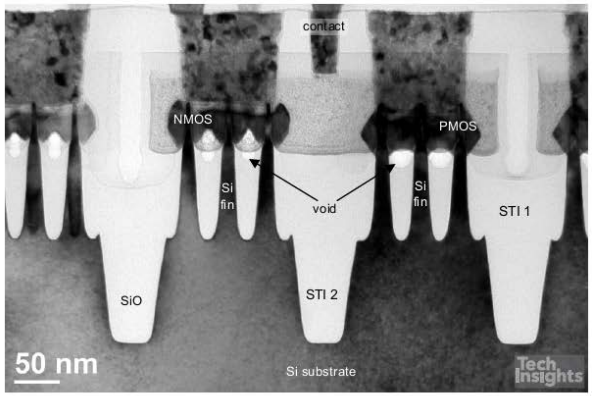
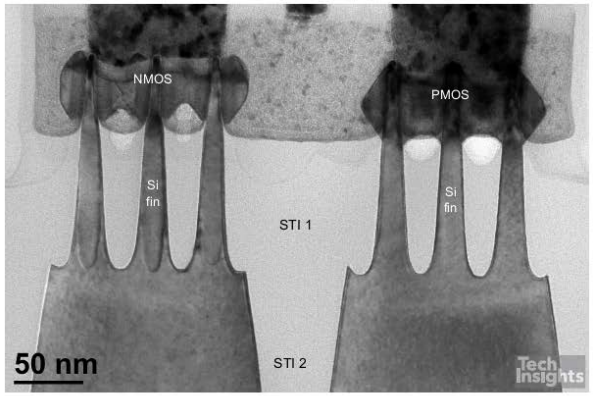
| Claim 6 | Accused Instrumentalities |
|---|---|
| The device as claimed in claim 1, wherein the contact resistance is reduced by selecting the size of a contact region which is in contact with said metal layer to be greater than the width of said Fin active region and/or the length of said gate. | The Accused Instrumentalities comprise a FinFET device, as claimed in claim 1, wherein the contact resistance is reduced by selecting the size of a contact region which is in contact with said metal layer to be greater than the width of said Fin active region and/or the length of said gate.<br><br>For example, in the Qualcomm Snapdragon 835, the size of a contact region which is in contact with the metal layer is greater than the width of the Fin active region, as shown below:[26]<br><br>  <br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/n-p sd 39k b_225176<br><br>  <br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/n-pmos sd 64k_225176<br><br>This design in the Samsung 10nm FinFET technology reduces the contact resistance. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| Claim 7 | Accused Instrumentalities |
|---|---|
| A double-gate FinFET device, comprising: | *See* Claim 1. |
| a bulk silicon substrate; | *See* Claim 1. |
| a Fin active region which is a wall-shape single crystalline silicon on a surface of the bulk silicon substrate and connected to said bulk silicon substrate; | *See* Claim 1. |
| a second oxide layer which is formed up to a certain height of the Fin active region from the surface of bulk silicon substrate; | *See* Claim 1. |
| a gate oxide layer which is formed on both side-walls of the Fin active region protruded from said second oxide layer; | *See* Claim 1. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| | |
|---|---|
| a first oxide layer which is formed on the upper surface of said Fin active region with a thickness greater or equal to that of the gate oxide; | *See* Claim 1. |
| a gate which is formed on said first and second oxide layer; | *See* Claim 1. |
| a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region; and | *See* Claim 1. |
| a contact region and a metal layer which are formed at said source/drain and gate contact region, | *See* Claim 1. |
| wherein the contact resistance is reduced by selecting the size of a contact region which is in contact with said metal | *See* Claim 1. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| | |
|---|---|
| layer to be greater than the width of said Fin active region, and/or the length of said gate, | |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

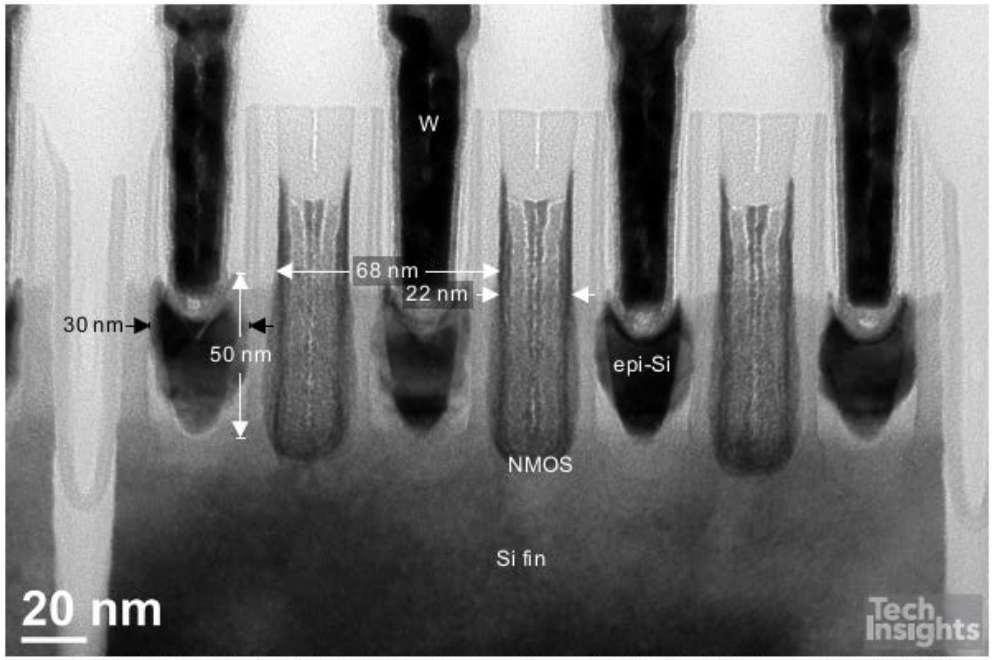
| | |
|---|---|
| and selective epitaxial layer is grown on both sides (source/drain region) of the Fin active region except where said Fin active region overlaps with the gate in a self-aligned manner to the gate, in order to reduce parasitic source/drain resistance. | The Accused Instrumentalities comprise a selective epitaxial layer grown on both sides (source/drain region) of the Fin active region except where said Fin active region overlaps with the gate in a self-aligned manner to the gate, in order to reduce parasitic source/drain resistance.<br><br>The selective epitaxial layers in the Qualcomm Snapdragon 835, for example, are shown below:[27]<br><br>  <br><br>4.TEM/TEM X-Section/Across the Transistor Gates/LOGIC/NMOS/gates__88k_225177<br><br>The epitaxial layers are located on both sides (source/drain region) of the Fin active region, except where the Fin active region overlaps with the gate, in a self-aligned manner to the gate. The use selective epitaxial layers in this manner reduces parasitic source/drain resistance. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| Claim 9 | Accused Instrumentalities |
|---|---|
| The device as claimed in claim 7, wherein said selective epitaxial layer is grown by depositing a dielectric layer, and anisotropically etching as much as the thickness of the dielectric layer and the height of the Fin active region protruding above the second oxide layer, and taking the silicon which is exposed at side-walls of the Fin active region except the vicinity where the Fin active region and gate meets and a poly-silicon gate, as seeds. | The Accused Instrumentalities comprise a FinFET device, as claimed in Claim 7, in which the selective epitaxial layer is grown by depositing a dielectric layer, and anisotropically etching as much as the thickness of the dielectric layer and the height of the Fin active region protruding above the second oxide layer, and taking the silicon which is exposed at the side-walls of the Fin active region except the vicinity where the Fin active region and gate meets and a poly-silicon gate, as seeds. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

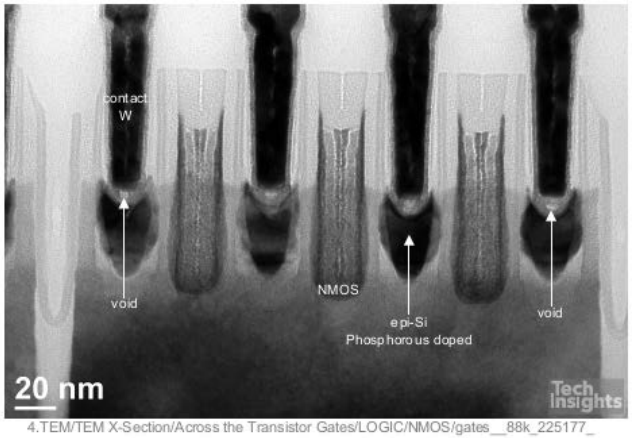
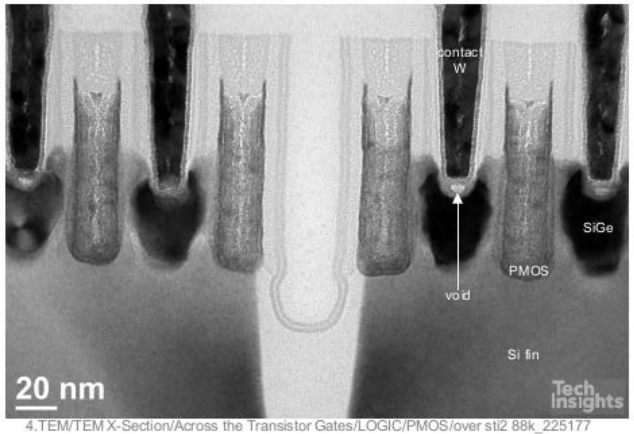
| Claim 10 | Accused Instrumentalities |
|---|---|
| The device as in any one of claims 7, wherein the material for said selective epitaxial layer is selected from the group consisting of a single crystalline silicon, single crystalline SiGe, single crystalline Ge, poly-silicon, and poly SiGe. | The Accused Instrumentalities comprise a FinFET device, as claimed in claim 7, in which the material for the selective epitaxial layer is selected from the group consisting of a single crystalline silicon, single crystalline silicon SiGe, single crystalline Ge, poly-silicon, and poly SiGe.<br><br>For example, in the Qualcomm Snapdragon 835, the material for the selective epitaxial layers is selected from the group consisting of a single crystalline silicon, single crystalline silicon SiGe, single crystalline Ge, poly-silicon, and poly SiGe:[28]<br><br>▪ Embedded strain technology is continued with merged silicon germanium (SiGe) epi for PMOS and merged Si epi (phosphorous doped) for NMOS<br><br>This is shown in the images below:[29]<br><br>  <br>4.TEM/TEM X-Section/Across the Transistor Gates/LOGIC/NMOS/gates__88k_225177_<br>  <br>4.TEM/TEM X-Section/Across the Transistor Gates/LOGIC/PMOS/over sti2 88k_225177 |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| Claim 11 | Accused Instrumentalities |
|---|---|
| The device as claimed in claim 1, wherein said doping junction depth for the source/drain formed in said Fin active region, when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to 50 nm above the reference level. | The Accused Instrumentalities comprise a FinFET device, as claimed in claim 1, in which the doping junction depth for the source/drain formed in said Fin active region, when the upper surface of the second oxide layer is taken as a reference level of 0 nm, is around 0 nm to 50 nm above the reference level. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| Claim 12 | Accused Instrumentalities |
|---|---|
| The device as claimed in claim 1, wherein said doping junction depth for the source/drain formed in said Fin active region, when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to −50 nm below the reference level. | The Accused Instrumentalities comprise a FinFET device, as claimed in claim 1, in which the doping junction depth for the source/drain formed in the Fin active region, when the upper surface of said second oxide layer is taken as a reference level of 0 nm, is around 0 nm to -50 nm below the reference level. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| Claim 13 | Accused Instrumentalities |
|---|---|
| A double-gate FinFET device, comprising: | *See* Claim 1. |
| a bulk silicon substrate; | *See* Claim 1. |
| a Fin active region which is a wall-shape single crystalline silicon on a surface of the bulk silicon substrate and connected to said bulk silicon substrate; | *See* Claim 1. |
| a second oxide layer which is formed up to a certain height of the Fin active region from the surface of bulk silicon substrate; | *See* Claim 1. |
| a gate oxide layer which is formed on both side-walls of the Fin active region protruded from said second oxide layer; | *See* Claim 1. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| | |
|---|---|
| a first oxide layer which is formed on the upper surface of said Fin active region with a thickness greater or equal to that of the gate oxide; | *See* Claim 1. |
| a gate which is formed on said first and second oxide layer; | *See* Claim 1. |
| a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region; and | *See* Claim 1. |
| a contact region and a metal layer which are formed at said source/drain and gate contact region, | *See* Claim 1. |
| wherein the resistance of said Fin active region is reduced by enlarging the width of said Fin active region within the oxidation | In the Accused Instrumentalities, the width of the Fin active region is enlarged as it approaches the bulk silicon substrate within the oxidation layer, reducing the resistance of the Fin active region.<br><br>For example, in the Qualcomm Snapdragon 835, this feature is shown in the image below:[30] |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

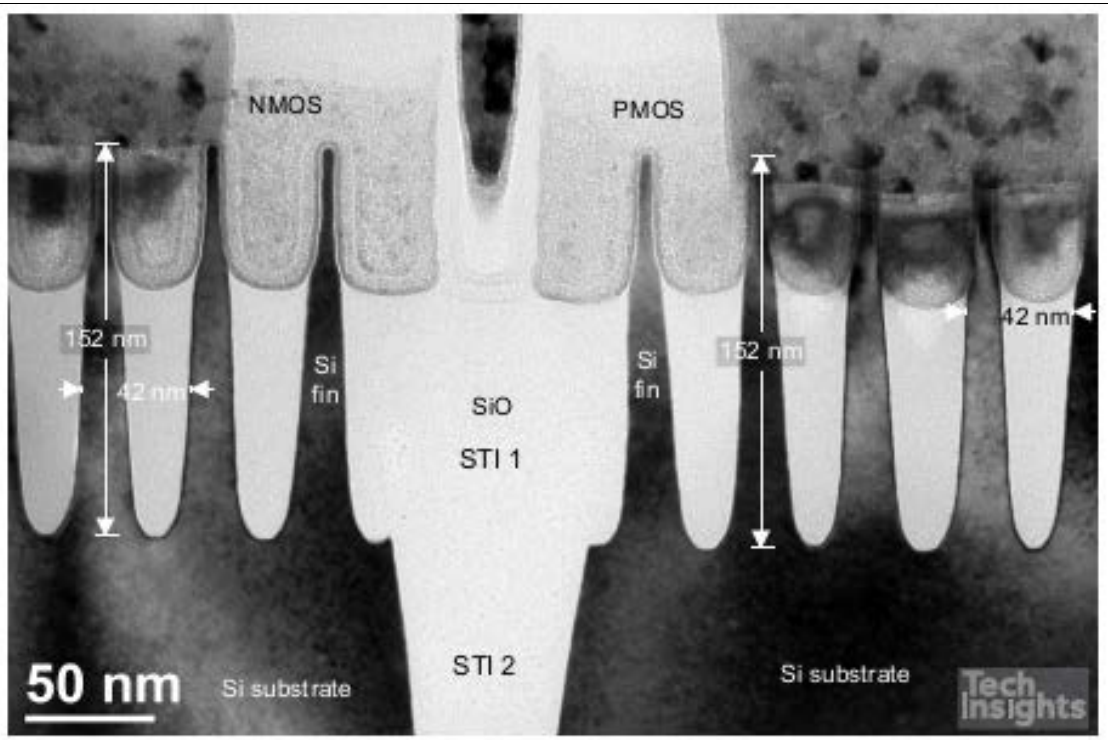
| | |
|---|---|
| layer as it approaches the bulk silicon substrate. |  <br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/n and pmos 64k_vg_225176<br><br>The width of the Fin active region increases as it approaches the bulk silicon substrate within the oxidation layer. This design in the Samsung 10nm FinFET technology reduces the resistance of the Fin active region. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

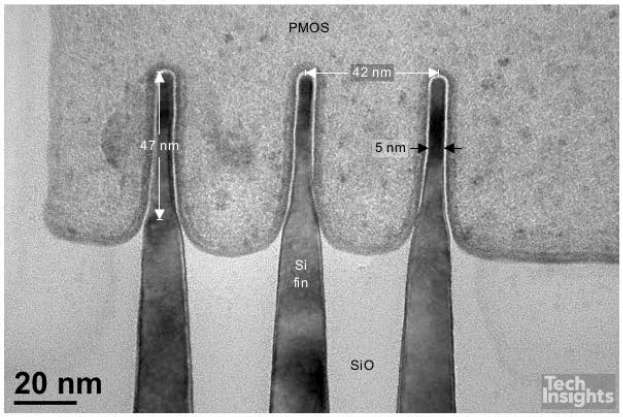
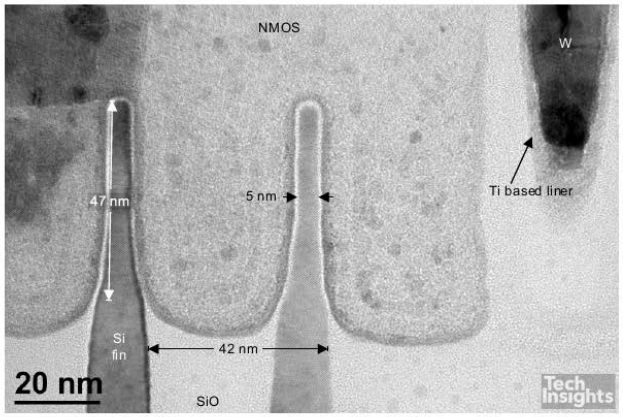
| Claim 15 | Accused Instrumentalities |
|---|---|
| The device as claimed in claim 1, wherein the two top corners of said Fin active region are chamfered through an oxidation and etching, or (and) annealing process in a hydrogen atmosphere. | The Accused Instrumentalities comprise a FinFET device, as claimed in claim 1, in which the top corners of the Fin active region are chamfered through oxidation and etching and/or annealing process in a hydrogen atmosphere<br><br>For example, in the Qualcomm Snapdragon 835, the two top corners of the Fin active region are chamfered, as shown below:[31]<br><br>PMOS<br>  <br><br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/pmos fins 130k_225176<br><br>NMOS<br>  <br><br>4.TEM/TEM X-Section/Across the Transistor Fins/LOGIC/nmos 180k g2_225176 |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| Claim 16 | Accused Instrumentalities |
|---|---|
| The device as claimed in claim 2, wherein the height of said Fin active region from the surface of said bulk silicon substrate lies in a range between 10 nm and 1000 nm. | *See* Claim 3. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| Claim 17 | Accused Instrumentalities |
|---|---|
| The device as claimed in claim 16, wherein the height of said Fin active region from the surface of said second oxide layer is between 5 nm and 300 nm. | *See* Claim 4. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

| Claim 19 | Accused Instrumentalities |
|---|---|
| The device as claimed in claim 9, wherein the material for said selective epitaxial layer is selected from the group consisting of a single crystalline silicon, single crystalline SiGe, single crystalline Ge, poly-silicon, and poly SiGe. | *See* Claim 10. |

**EXHIBIT B**
**Infringement Chart for U.S. Patent No. 6,885,055**

[1] *10nm FinFET and Multi-Patterning Technology - Evolution Continues*, SAMSUNG FOUNDRY (last visited Feb. 6, 2019), https://www.samsungfoundry.com/foundry/homepage/anonymous/technology12inch10nm.do.

[2] *Id.*

[3] *The Easy Guide to a Semiconductor: Why the 10nm FinFET Process?*, SAMSUNG (May 10, 2017), https://www.samsung.com/semiconductor/minisite/exynos/newsroom/blog/the-easy-guide-to-a-semiconductor-why-the-10nm-finfet-process/.

[4] *Samsung-GLOBALFOUNDRIES 14nm Collaboration*, SAMSUNG & GLOBALFOUNDRIES (Apr. 2014), https://www.globalfoundries.com/sites/default/files/samsung-globalfoundries-14nm-overview-presentation.pdf, at 4.

[5] *Qualcomm and Samsung Collaborate on 10nm Process Technology for the Latest Snapdragon 835 Mobile Processor*, QUALCOMM (Nov. 17, 2016), https://www.qualcomm.com/news/releases/2016/11/17/qualcomm-and-samsung-collaborate-10nm-process-technology-latest-snapdragon.

[6] TECHINSIGHTS, *Qualcomm Snapdragon 835 MSM8998 Samsung 10LPE FinFET Process* ("TECHINSIGHTS") at 5-6.

[7] TECHINSIGHTS at 4.

[8] TECHINSIGHTS at 23.

[9] *Inside of 10nm Technology Node*, MATERIAL SCIENCE SERVICE (Mar. 2018), http://www.semiconchina.org/Semicon_China_Manager/upload/kindeditor/file/20180320/20180320111103_783.pdf, at 9.

[10] TECHINSIGHTS at 15.

[11] TECHINSIGHTS at 23.

[12] TECHINSIGHTS at 26.

[13] TECHINSIGHTS at 23.

[14] TECHINSIGHTS at 30.

[15] TECHINSIGHTS at 30.

[16] TECHINSIGHTS at 33.

[17] TECHINSIGHTS at 25, 26.

[18] TECHINSIGHTS at 38-40.

[19] TECHINSIGHTS at 31.

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**Infringement Chart for U.S. Patent No. 6,885,055**

[20] TECHINSIGHTS at 5.

[21] TECHINSIGHTS at 24.

[22] TECHINSIGHTS at 23.

[23] TECHINSIGHTS at 5.

[24] TECHINSIGHTS at 24.

[25] TECHINSIGHTS at 23.

[26] TECHINSIGHTS at 36.

[27] TECHINSIGHTS at 26.

[28] TECHINSIGHTS at 6.

[29] TECHINSIGHTS at 37.

[30] TECHINSIGHTS at 23.

[31] TECHINSIGHTS at 24.